Hardware Implementation
Implementation results

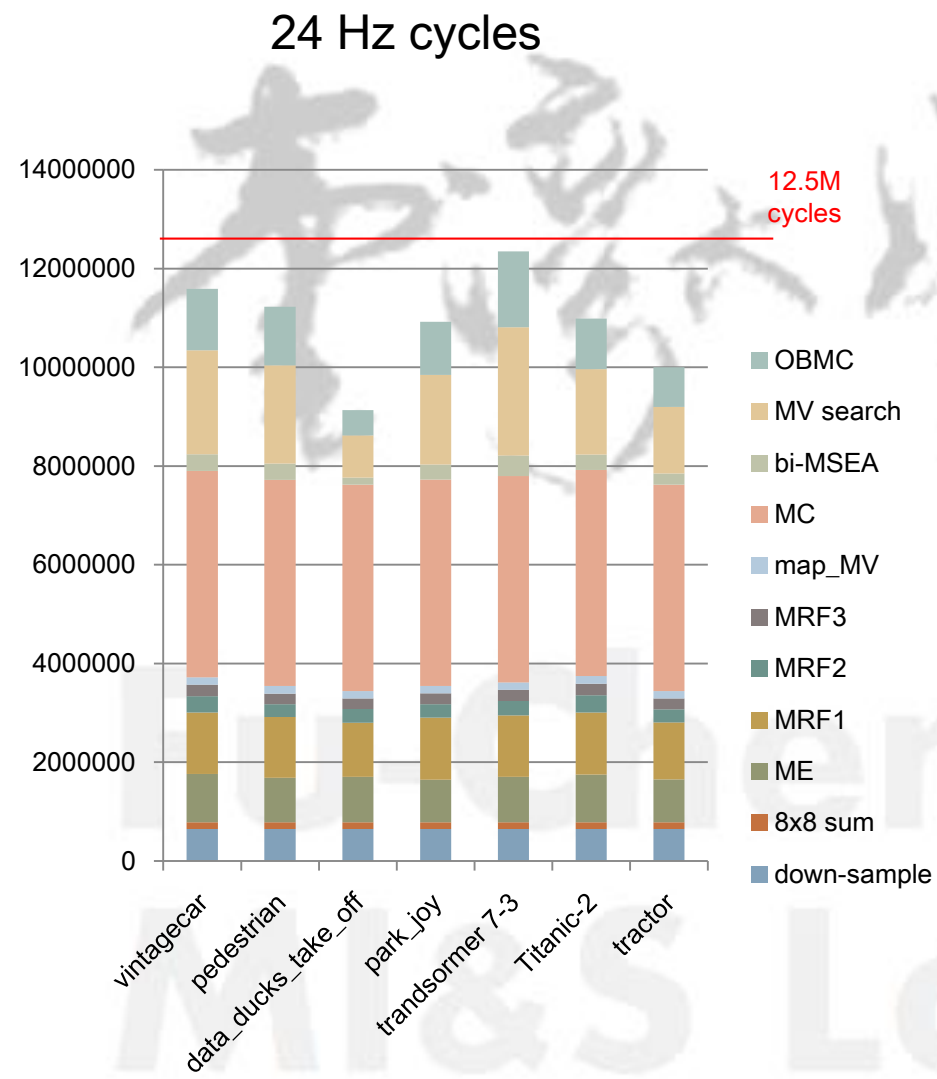
- Specification

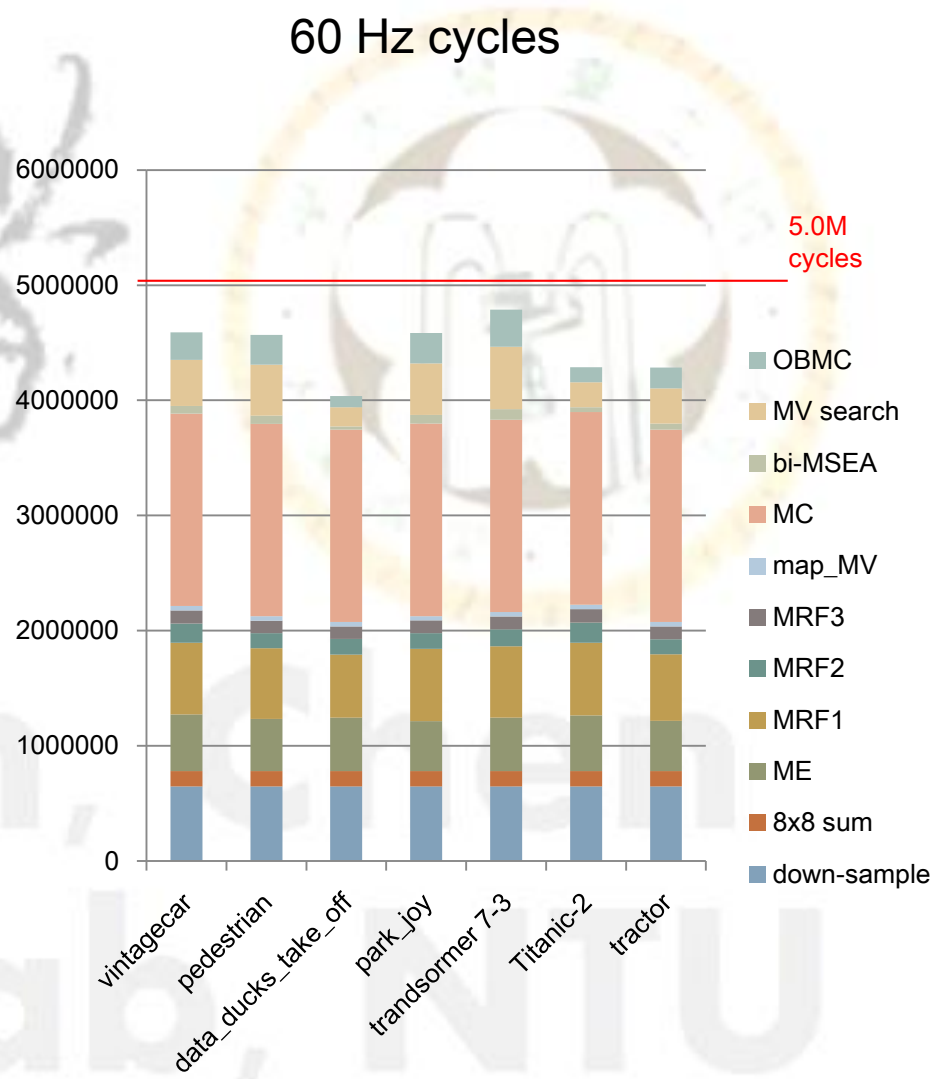
Design Specification	
Technology	UMC 90nm
Clock rate	300MHz
Bus width	128 bits/cycle
DRAM	DDR3-1333
Gate count with SRAM	537652
Gate count without SRAM	273845
SRAM size	9984 Bytes single port

Capability Specification	
FRUC mode	24 Hz -> 120 Hz 60 Hz -> 120 Hz
Frame size	3840x2160
Search range	±128 x ±128

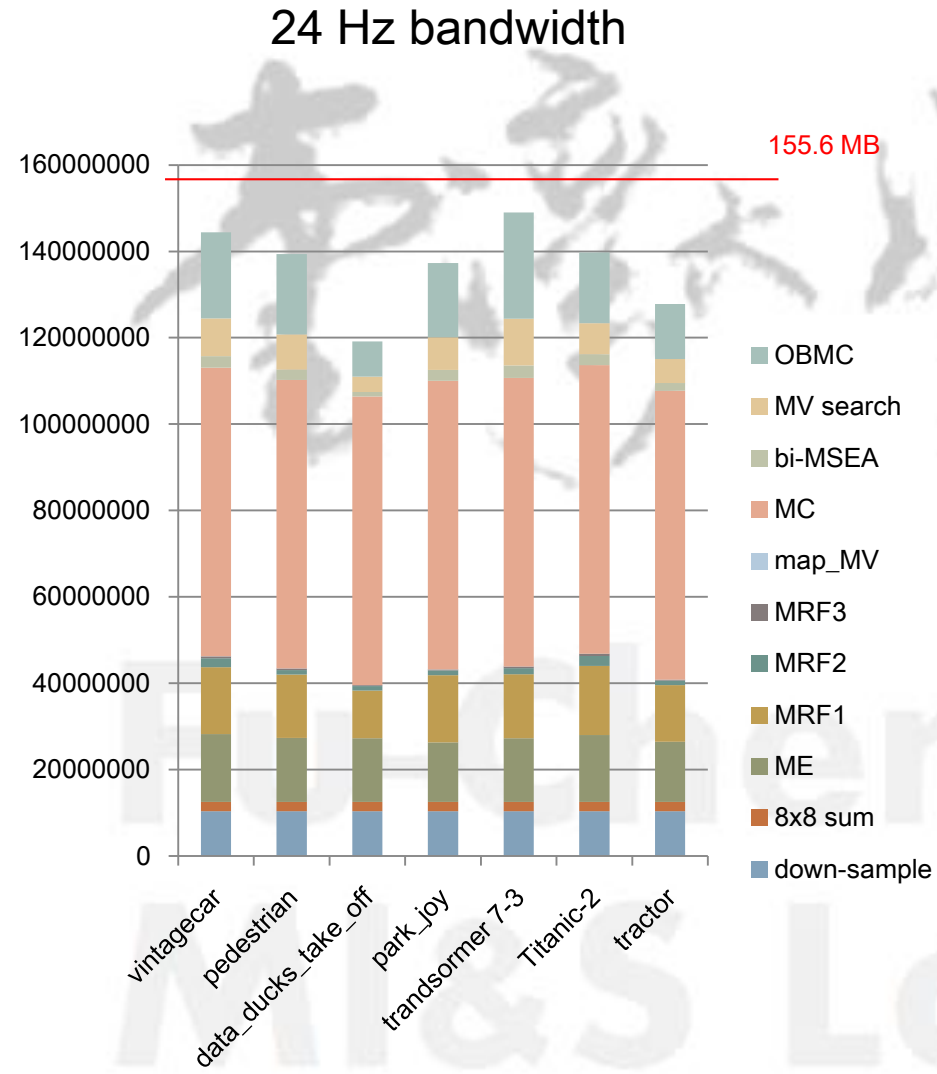
- Algorithm vs. hardware
  - Raster scan ⟶ two-way scan
  - MV search ±8 x ±8 ⟶ ±8 x ±8 on even points

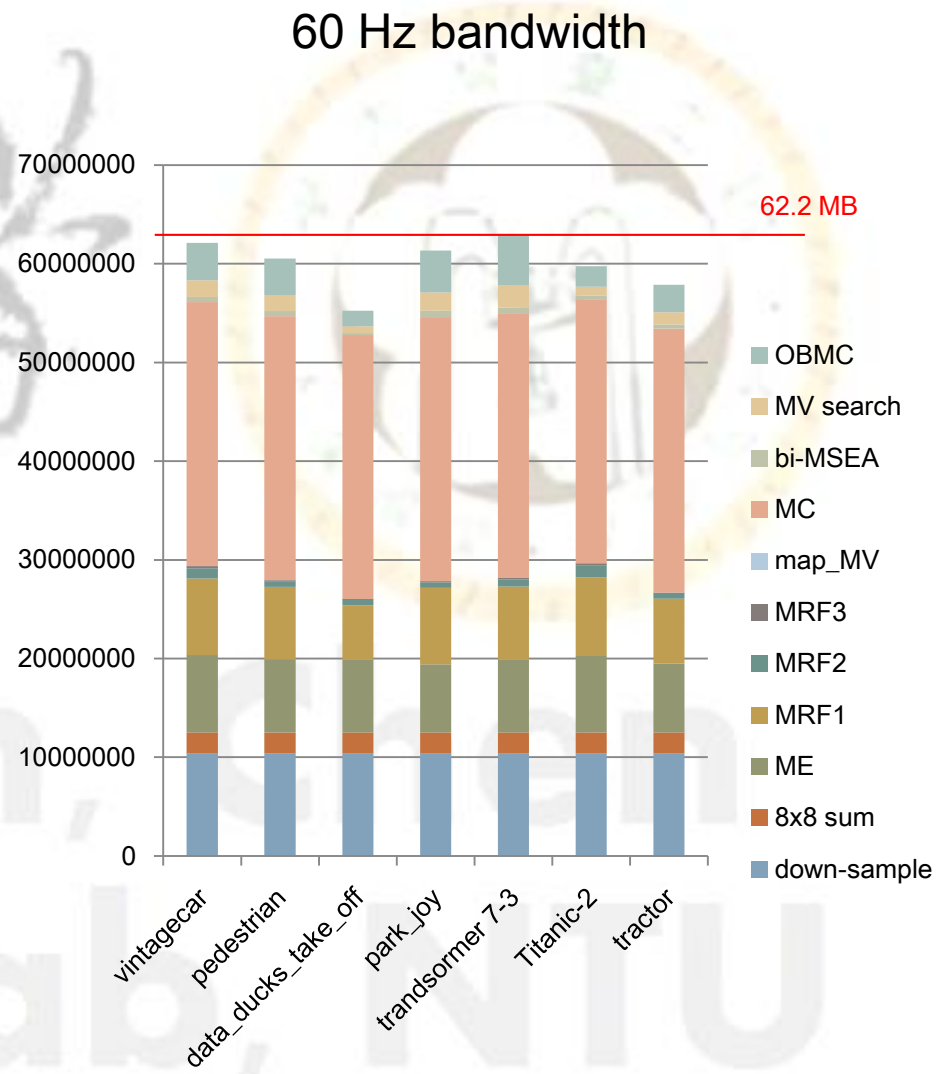
Experimental Results
Cycles & Bandwidth Consumption





Experimental Results
Cycles & Bandwidth Consumption





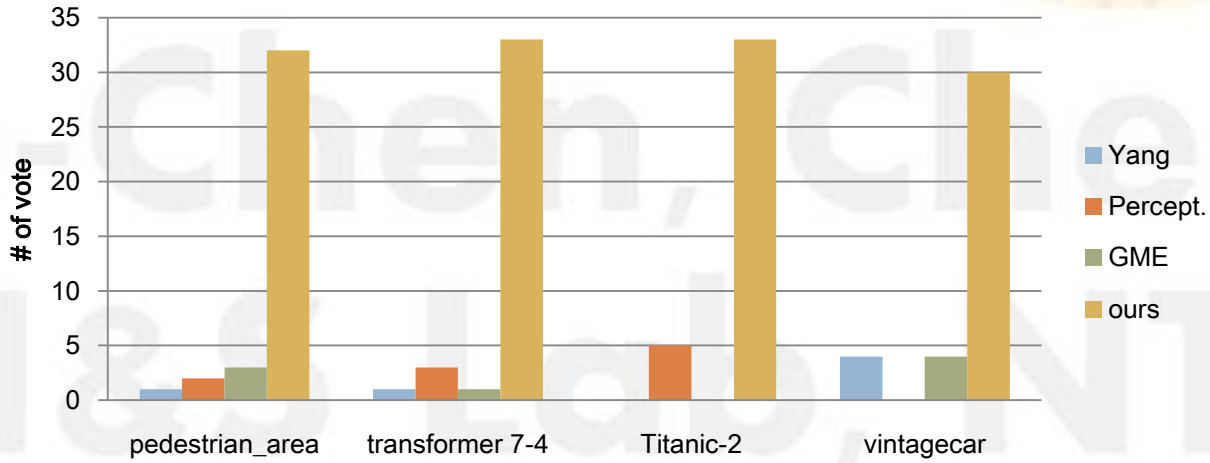
Experimental Results – Evaluation
The Comparison

- Selected papers
  - [Yang 07]
    - Extracting MV from JM 15.1
    - OBME + OBMC
    - No hardware implementation
  - [Percept.10]
    - Extracting MV from JM 15.1
    - Ignore MVs that are perceptually unapparent
    - 60 Hz -> 120 Hz, 1080p
  - [GME 08]
    - Global motion estimation
    - Sub-block division
    - 60 Hz -> 120 Hz, 1080p

Experimental Results – Evaluation
Subjective evaluation

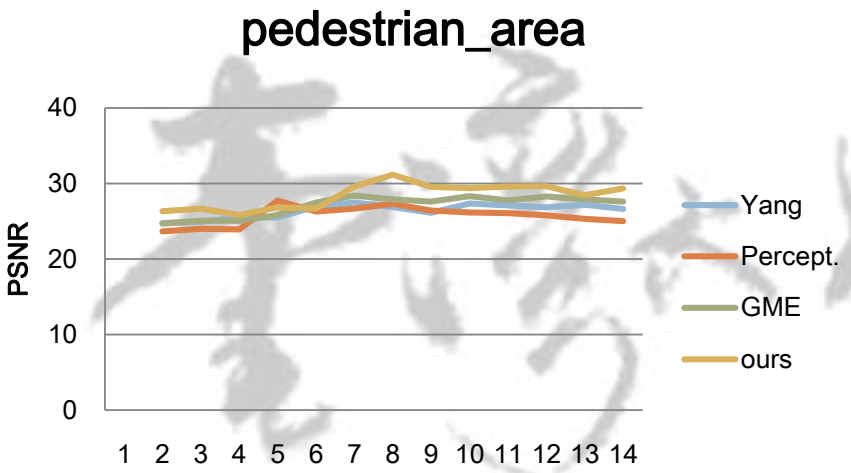
- Subjects
  - 38 people
    - 22 people come from NTU's EE students
    - 16 people come from internet
- Experimental method
  - Watch twice up-converted 1080p sequences of 4 algorithms frame by frame at the same time

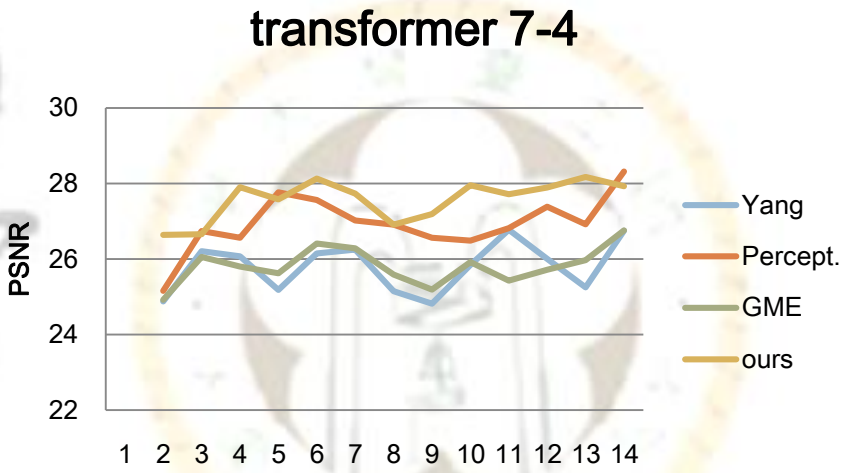
  - Select the best one among 4 algorithms for each sequence

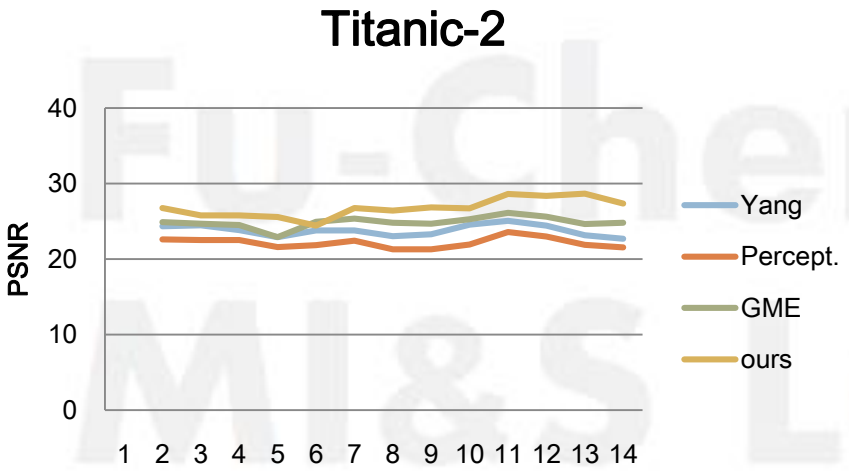


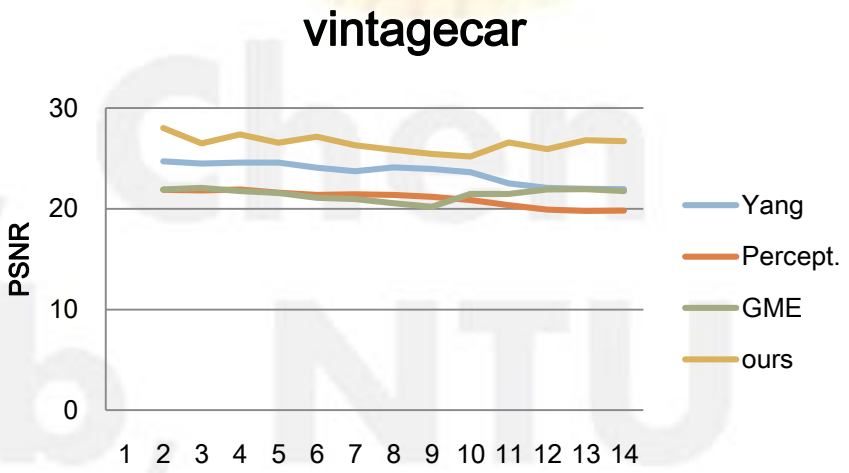
Experimental Results – Evaluation

Objective evaluation



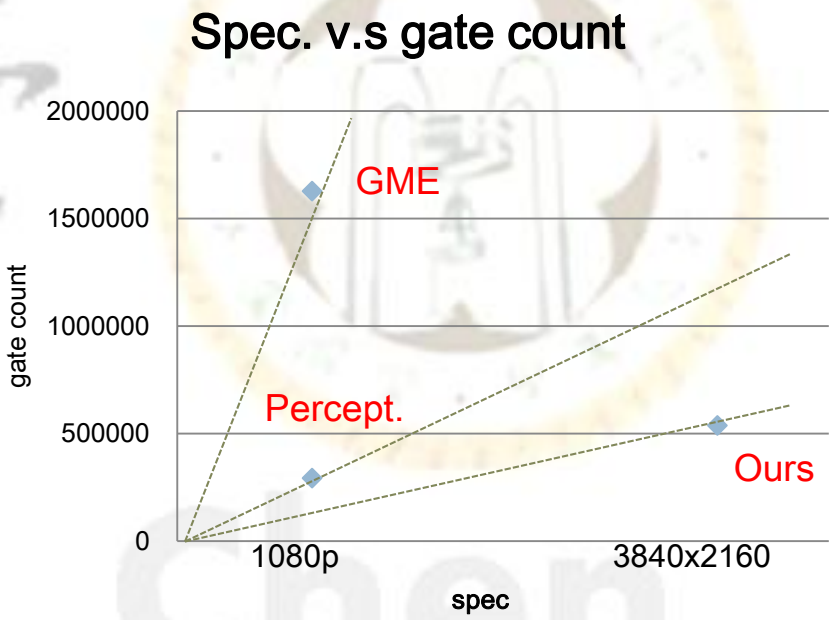






Experimental Results – Evaluation
Hardware efficiency evaluation

	Percept.	GME	Ours
Technology	UMC 90nm	UMC 90nm	UMC 90nm
Clock rate	200MHz	133MHz	300MHz
Gate count with SRAM	292732*	1627900*	537652
Gate count without SRAM	212582	1301464	273845
SRAM size (Byte)	3036*	12365*	9984
FRUC mode	60Hz -> 120Hz	60Hz -> 120Hz	24Hz -> 120Hz 60Hz -> 120Hz
Frame size	1920x1080	1920x1080	3840x2160



*Assume single port SRAM with 3.3 gate count / bit

Conclusion

- FRUC algorithm
  - Low-cost ICM for MRF
    - 65536 → 9 MRF energy computation
  - Block based through MC
    - Better than 3 general methods
  - Precise artifact detection
    - 100% → 12% sub-blocks
  - Artifact-reduction post-processing
    - Reduce block artifact
    - Consider occlusion

Conclusion

- FRUC architecture
  - Flexible sum-trees
    - 341 → 85 adders
    - Shared by other modules
  - Ping-pong two-way scan order
    - Eliminate the dependency
    - Data pre-fetch
  - MV grouping
    - 1536 → 459 cycle / block
    - 48M → 8.6 MB bandwidth
  - Inverse-MC scheduling
    - 6.2M → 4.0 M cycles
    - 99.5M → 64.8 MB bandwidth
- Implementation results
  - Excellent hardware efficiency
    - Quad HD 3840x2160
    - 24Hz to 120Hz & 60Hz to 120Hz up-conversion
    - 274K gate count & 10KB single-port SRAM

Future work

- Scene change detection
  - Ex. Threshold on MRF energy
- Smaller block size for more detailed presentation
- Perceptual criteria for post-processing
- Handle the region with multi-motion

- The modeling-based FRUC
  - Modeling the inter-frame
  - Finding motions, occlusion labels, pixel values of inter-frame s.t. energy is minimized